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From:	Joseph T. Cygan	**Sender's Ext.:**	312-609-7945
Date:	June 3, 2009	**Total Pages:**	12 (including this page)
Client No.: 00100.03.0040		**Time Received by Fax Dept.:**	

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Dear Examiner Wang,

Please see attachment.

Best regards,
Joseph Cygan

DRAFT ONLY – PROPOSED AMENDMENT

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Rubin, Norman, et al.
Serial No.: 10/767,480
Filing Date: January 28, 2004
Confirmation No.: 5073

Examiner: Wang, Ben C.
Art Unit: 2192
Atty. Docket No.: 00100.03.0040

Title: **METHOD AND APPARATUS FOR STATIC SINGLE ASSIGNMENT FORM DEAD CODE ELIMINATION**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Dear Sir:

In response to an Examiner Interview of June 1st, 2009, please amend the above identified patent application in accordance with the following:

Amendments to the Claims beginning on page 2 of this paper; and

Remarks/Arguments beginning on page 10 of this paper which include a **Summary of the Examiner Interview** of June 1st, 2009.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for static single assignment form dead code elimination, the method comprising:

examining a first instruction of a machine code off of a worklist in memory, wherein the first instruction includes a previous link and a write mask, wherein said write mask includes a bit corresponding to a component produced by said first instruction;

examining at least one second instruction, wherein the at least one second instruction is a source of the first instruction and wherein each of the at least one second instruction includes a previous link and a second write mask, wherein said second write mask includes a bit corresponding to a component produced by said second instruction;

determining, using said previous link of said at least one second instruction, if any components within a particular field of the at least one second instruction are required, wherein said previous link of said second instruction links said second instruction with a prior instruction that writes at least one component of said components;

when no components of the at least one second instruction are required, deleting the at least one second instruction from the machine code; and

when any component of the at least one second instruction is required, adding the at least one second instruction to the worklist in the memory.

2. (Original) The method of claim 1 further comprising:

generating the worklist by:

for each of a plurality of instructions, determining if the instruction is a critical instruction; and

if the instruction is a critical instruction, writing the instruction to the worklist.

3. (Original) The method of claim 2 further comprising:

setting a live bit for each component of the plurality of instructions.

4. (Previously Presented) The method of claim 2 wherein each critical instruction is an instruction that generates an export value.

5. (Previously Presented) The method of claim 2 further comprising:

prior to generating the worklist:

receiving a plurality of instructions;

adding to each instruction the previous link; and

adding to each instruction the write mask.

6. (Original) The method of claim 5 wherein the write mask is a multi-bit field representing a number of components in a superword register.

7. (Previously Presented) The method of claim 6 wherein each of the plurality of instructions are written to the worklist a predetermined number of times, wherein the predetermined number of times is based on the number of components in the superword register.

8. (Currently Amended) A method for static single assignment form dead code elimination comprising:

receiving a plurality of instructions;

adding to each instruction a previous link, wherein said previous link links said each instruction with a prior instruction that writes at least one component;

adding to each instruction a write mask, wherein said write mask includes a bit corresponding to a component produced by said each instruction; and

generating a worklist in memory by:

for each of the plurality of instructions, determining if the instruction is a critical instruction; and

if the instruction is a critical instruction, writing the instructions to the worklist in the memory.

9. (Previously Presented) The method of claim 8 further comprising:

setting a live bit for each component of the plurality of instructions;

examining a first instruction off of the worklist;

examining at least one second instruction in the machine code, wherein the at least one second instruction is a source of the first instruction;

determining if any component within a particular field of the at least one second instruction is live; and

when no components of the at least one second instruction are live, deleting the second instruction from the worklist.

10. (Cancelled)

11. (Previously Presented) The method of claim 8 wherein each critical instruction is an instruction that generates an export value.

12. (Original) The method of claim 8 wherein the write mask is a multi-bit field representing a number of components in a superword register.

13. (Previously Presented) The method of claim 12 wherein each of the plurality of instructions are written to the worklist a predetermined number of times, wherein the predetermined number of times is based on the number of components in the superword register.

14. (Currently Amended) An apparatus for static single assignment form dead code elimination comprising:

at least one memory device storing a plurality of executable instructions of a machine code; and

at least one processor operably coupled to the at least one memory device, operative to receive the plurality of executable instructions such that the at least one processor, in response to the plurality of executable instructions is further operative to:

examine a first instruction off of a worklist, wherein the first instruction includes previous link and a write mask, wherein said write mask includes a bit corresponding to a component produced by said first instruction;

examine at least one second instruction of the machine code, wherein the at least one second instruction is a source of the first instruction and each of the at least one second instruction includes a previous link and a second write mask, wherein said second write mask includes a bit corresponding to a component produced by said second instruction;

determine, using said previous link of said at least one second instruction, if any component within a particular field of the at least one second instruction is live, wherein said previous link of said second instruction links said second instruction with a prior instruction that writes at least one component of said components; and

when no components are live, delete the second instruction from the machine code.

15. (Previously Presented) The apparatus of claim 14 wherein the at least one processor in response to the plurality of instructions executable instructions is further operative to :

generate the worklist by:

for each of a plurality of instructions, determining if the instruction is a critical instruction; and

if the instruction is a critical instruction, writing the instruction to the worklist.

16. (Previously Presented) The apparatus of claim 15 wherein each critical instruction is an instruction that generates an export value.

17. (Cancelled)

18. (Previously Presented) The apparatus of claim 15 further comprising:

a superword register operably coupled to the at least one processor, wherein the write mask is a multi-bit field representing a number of components in the superword register.

19. (Currently Amended) An apparatus for static single assignment form dead code eliminations comprising:

at least one memory device storing a plurality of executable instructions of a machine code; and

at least one processor operably coupled to the at least one memory device, operative to receive the plurality of executable instructions such that the at least one processor, in response to the executable instructions is further operative to:

receive a plurality of instructions;

add to each instruction a previous link, wherein said previous link links said each instruction with a prior instruction that writes at least one component;

add to each instruction a write mask, wherein said write mask includes a bit corresponding to a component produced by said each instruction; and

generate a worklist by:

for each of the plurality of instructions; determining if the instruction is a critical instruction; and

if the instruction is a critical instruction, writing the instructions to the worklist;

examine a first instruction off of the worklist;

examine at least one second instruction from the machine code, wherein the at least one second instruction is a source of the first instruction;

determine, using a previous link of said at least one second instruction, if any component within a particular field of the at least one second instruction is live; and

when no component is live, delete the second instruction from the machine code.

20. (Original) The apparatus of claim 19 further comprising:

a superword register operably coupled to the at least one processor, wherein the write mask is a multi-bit field representing a number of components in a superword register.

21. (Previously Presented) The apparatus of claim 15, wherein the at least one processor in response to the plurality of executable instructions is further operative to set a live bit for each component of the plurality of instructions.

22. (Previously Presented) The method of claim 9, further comprising:

when any component of the at least one second instruction is live, adding the at least one second instruction to the worklist.

23. (Previously Presented) The apparatus of claim 14, wherein the at least one processor in response to the plurality of instructions executable instructions is further operative to :

when any component of the at least one second instruction is live, add the at least one second instruction to the worklist.

24. (Previously Presented) The apparatus of claim 19, wherein the at least one processor in response to the plurality of instructions executable instructions is further operative to :

when any component of the at least one second instruction is live, add the at least one second instruction to the worklist.

REMARKS

Claims 1-5, 8, 9, 11, 14-16, 19 and 21-24 are pending in the application. Claims 6-7, 12-13, 18, and 20 are allowable but objected to for depending upon rejected base claims. Applicants submit the instant Supplemental Amendment in response to an Examiner Interview. Claims 1, 8, 14 and 19 are hereby amended.

Summary of the Examiner Interview of June 1, 2009

An Examiner Interview was conducted telephonically on June 1, 2009 between Examiner Ben C. Wang and Applicants' representative, Joseph T. Cygan (Reg. No. 50,937). Applicants thank the Examiner for the courtesy of the phone call and for taking time to discuss the application.

The independent claims 1, 8, 14 and 19 have been amended to clarify the purpose of the write mask as discussed by the Examiner and Applicants' representative during the June 1st phone call.

Therefore Applicants respectfully submit that the claims are in condition for allowance.

CONCLUSION

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. Also, no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant(s) has/have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

It is submitted that the claims clearly define the invention, are supported by the specification and drawings, and are in a condition for allowance. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. Should the Examiner have any questions or concerns that may expedite prosecution of the present application, the Examiner is encouraged to telephone the undersigned

Respectfully submitted,

Date: June 3, 2009

By: / /
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Registration No. 50,937

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